WHAT IS CLAIMED IS:

1. An image processing apparatus comprising:

a block expanding section formed in a semiconductor chip, which handles an area to be drawn in units of blocks each composed of a plurality of pixels, and performs expansion calculation of information on a representative point of each block; and

a plurality of pixel processing sections formed in the semiconductor chip, each of said plurality of pixel processing sections comprises: a pixel expanding section which receives block representative point information calculated in the block expanding section and expands information in units of pixels at least in a rectangular area from the information; and a computing section which receives information expanded by the pixel expanding section and performs computation in units of pixels from the information, each of said plurality of pixel processing sections performs graphics processing in cooperation with the block expanding section, and performs image processing independent of the block expanding section.

2. The image processing apparatus according to claim 1, wherein the pixel expanding section comprises:

a loop counter section which controls counting of a multiple loop;

a buffer;

a buffer address calculating section connected to the loop counter section and the buffer, which calculates an address for reading data from the buffer; and

an address and parameter calculating section connected to the buffer, which reads data from the buffer and calculates a plurality of parameters and memory addresses required for the computing section.

3. The image processing apparatus according to claim 1, wherein the computing section comprises:

a plurality of product sum calculating sections which perform computation using data read from a memory inside or outside the image processing apparatus in accordance with a plurality of addresses calculated by the pixel expanding sections and a plurality of parameters calculated by the pixel expanding section; and

an accumulator added at the final stage of the product sum calculating sections, which performs accumulation instead of data reading from the memory.

4. The image processing apparatus according to claim 3, wherein each of said plurality of pixel processing sections further comprises a First-in First-out buffer circuit which is connected to the computing section and from/into which data is written into/read from the computing section.

5. The image processing apparatus according to

claim 3, wherein each of said plurality of pixel processing sections further comprises a buffer circuit which is connected to the pixel expanding section and the computing section, into which data is written from the computing section, and from which data is read into the pixel expanding section.

6. The image processing apparatus according to claim 3, wherein each of said plurality of pixel processing sections further comprises a buffer circuit which is connected to the pixel expanding section and the computing section, and which has a first pass into which data is written from the computing section and from which data is read into the pixel expanding section and a second pass from which data is read into the computing section in accordance with an address from the pixel expanding section.

7. An image processing apparatus comprising:

a plurality of image processing sections, each of said plurality of image processing sections comprises:

a block expanding section formed in a semiconductor chip, which handles an area to be drawn in units of blocks each composed of a plurality of pixels, and performs expansion calculation of information on a representative point of each block; and

a plurality of pixel processing sections formed in the semiconductor chip, each of said plurality of pixel

processing sections includes: a pixel expanding section which receives block representative point information calculated in the block expanding section and expands information in units of pixels at least in a rectangular area from the information; and

a computing section which receives information expanded by the pixel expanding section and performs computation in units of pixels from the information, each of said plurality of pixel processing sections performs graphics processing in cooperation with the block expanding section, and performs image processing independent of the block expanding section, and each of said plurality of image processing sections simultaneously performs processings different from each other.

8. An image processing apparatus comprising:

a pixel expanding section formed in a semiconductor chip, which handles an area to be drawn in units of blocks each composed of a plurality of pixels and calculates a representative value of each pixel in each block; and

a plurality of pixel processing sections formed in the semiconductor chip, each of said plurality of pixel processing sections comprises: an address calculating section which receives a pixel representative value calculated in the pixel expanding section and calculates a parameter and an address of a pixel at

least in a rectangular area; and a computing section which receives an address calculated in the address calculating section and performs partial computation of pixel processing using data read from a memory according to the address, each of said plurality of pixel processing sections performs graphics processing in cooperation with the pixel expanding section, and performs image processing independent of the pixel expanding section.

9. The image processing apparatus according to claim 8, wherein each of said plurality of pixel processing sections further comprises a First-in First-out buffer circuit which is connected to the computing section and from/into which data is written into/read from the computing section.

10. The image processing apparatus according to claim 8, wherein each of said plurality of pixel processing sections further comprises a buffer circuit which is connected to the pixel expanding section and the computing section, into which data is written from the computing section, and from which data is read into the pixel expanding section.

11. The image processing apparatus according to claim 8, wherein each of said plurality of pixel processing sections further comprises a buffer circuit which is connected to the pixel expanding section and the computing section and which has a first pass into

which data is written from the computing section and from which data is read into the pixel expanding section and a second pass from which data is read into the computing section according to an address from the pixel expanding section.

12. An image processing apparatus comprising:

a plurality of image processing sections, each of said plurality of image processing sections comprises:

a pixel expanding section formed in a semiconductor chip, which handles an area to be drawn in units of blocks each composed of a plurality of pixels and calculates a representative value of each pixel in each block; and

a plurality of pixel processing sections formed in the semiconductor chip, each of said plurality of pixel processing sections includes: an address calculating section which receives a pixel representative value calculated in the pixel expanding section and calculates a parameter and an address of a pixel at least in a rectangular area; and a computing section which receives an address calculated in the address calculating section and performs partial computation of pixel processing using data read from a memory according to the address, each of said plurality of pixel processing sections performs graphics processing in cooperation with the pixel expanding section, and performs image processing independent of the pixel

expanding section, and each of said plurality of image processing sections simultaneously performs processings different from each other.